

REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

Disposition of Claims

Claims 1-7 are pending in this application. Claims 1 and 5 are independent. The remaining claims depend, directly or indirectly, from claims 1 and 5.

Drawings

In response to the drawing objections in the Examiner's previous Office Action of December 3, 2003, Applicant submitted drawing corrections to Figure 1. Applicant notes that the current Office Action does not indicate whether the drawings are accepted and the objection is withdrawn. Applicant respectfully requests that the Examiner accept the drawing filed in response to the Office Action of December 3, 2003 and withdraw any objections to the drawings.

Acknowledgement of Priority

Applicant has amended the specification to claim priority to French Patent Application No. 99/00858, filed on January 27, 1999. Applicant respectfully requests acknowledgement of this claim for priority.

Rejections under 35 U.S.C. § 103

Claims 1-3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,774,633 ("Dehaine"). This rejection is respectfully traversed.

The present invention relates to an integrated circuit (IC) device, which includes an active chip and a complementary chip attached to the active chip. The active chip has an active face with a plurality of electrical connection terminals and a specified thickness (*i.e.*, 100 micrometers). Specifically, the complementary chip has a face that is attached to the active face of the active chip and has a larger thickness than the active chip. Thus, both faces are not only linked by electrical contacts, but actually are attached *face-to-face*, as recited in independent claim 1 of the present invention. Further, the complementary chip includes a plurality of

recesses, where each recess extends through the entire thickness of the complementary chip, from above a contact terminal to a side surface of the complementary chip (see, *e.g.*, page 3 of the specification). With the present invention, it is possible to provide an IC device permitting the manufacturing of an electronic unit for smart cards having a reduced thickness, while maintaining sufficient mechanical strength of the electronic unit. The plurality of recesses in the complementary chip, and the location of these recesses, provide the active chip with electrical connection as well as maintain the electronic unit of reduced thickness.

Dehaine discloses a method for assembling an integrated circuit on a substrate and the mounting of the device produced to a card having electronic microcircuits. The device includes a package containing a substrate, a chip, and contacts. The substrate used in Dehaine is a thin sheet of electrically insulating material, where the face of the substrate is largely covered by a metal layer including the contacts of the package. The metal layer is cut to form contacts that overlay a chip contact or connection element. However, Dehaine fails to disclose or suggest that the complementary chip has a face that is *attached to* the active face of the active chip, as required in independent claim 1 of the present invention. The Examiner references Figure 1 of Dehaine in asserting that Dehaine discloses this limitation of the present invention. As noted above, in the present invention, the active face of the active chip and the first face of the complementary chip of the present invention are not only electrically connected via contacts, but they are physically attached face-to-face. Figure 1 of Dehaine does not show or suggest this limitation.

Moreover, Dehaine fails to disclose or suggest that the recesses associated with the complementary chip extend in height through the entire thickness of the complementary chip and extend transversely from above a contact terminal to a side surface of the complementary chip as required by independent claim 1. In fact, neither Figure 1 of Dehaine nor the accompanying description of Figure 1 of Dehaine clearly indicates any dimensional information with respect to recesses (*i.e.*, contacts). Thus, it is clear that Dehaine does not teach or suggest the claimed invention.

Further, Applicant disagrees with the Examiner's assertion that thickness parameters with respect to semiconductor devices are subject to routine experimentation and optimization and therefore render the claimed invention obvious. The present invention does not specify thickness

as simply a number; rather, the thickness relates to the overall structure of the integrated circuit, and the overall thickness of the structure is obtained using the thickness of both the active chip and the complementary chip (see, *e.g.*, page 5 and page 6 of the specification). The thickness of the active chip specified in the claimed invention (*i.e.*, less than 100 micrometers) and the specific limitation that the complementary chip has a greater thickness than the active chip is the result of an applied manufacturing method specifically designed to obtain a thinner overall structure while maintaining the mechanical strength of the device. Thus, the focus of the thickness parameters specified in the present application is deliberate and significant, and not a matter of routine experimentation. Dehaine, as admitted by the Examiner, does not specify that the complementary chip has a greater thickness than the active chip. This is because Dehaine does not target using thickness parameters that maintain a sufficient mechanical strength of the overall structure.

In view of the above, it is clear that Dehaine does not render claim 1 of the present invention obvious. Thus, claim 1 is patentable over Dehaine. Further, dependent claims 2-4 are patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 4 stands rejected under 35 U.S.C. 103(a) as unpatentable over Dehaine in view of U.S. Patent No. 5,155,068 ("Tada"). This rejection is respectfully traversed. Claim 4 is dependent on independent claim 1. As described above, Dehaine does not disclose or suggest the invention as claimed in independent claim 1. Further, Tada fails to disclose or suggest that which Dehaine lacks.

Tada discloses a method for manufacturing an IC module for an IC card, where the IC module includes a large scale integration (LSI) chip that is thinned by a material removal technique. Specifically, Tada does not disclose or suggest that the complementary chip's first face is attached to the active face of the active chip in the manner described in the claimed invention. Further, Tada teaches a manufacturing technology using bump electrodes where the substrate is under the active device and the connecting terminal is over the bump electrodes. Thus, it is not possible for the substrate disclosed in Tada to include recesses, as required by claim 1 of the present invention. Therefore, Tada necessarily cannot and does not disclose that the complementary chip includes recesses extending through the entire thickness of the

complementary chip. In view of the above, claim 4 is patentable over Dehaine and Tada, whether considered separately or in combination. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 5-7 stand rejected under Dehaine in view of Admitted Prior Art (“APA”). This rejection is respectfully traversed. The Examiner asserts that Dehaine teaches the invention as claimed in claim 1. However, as described above, it is clear that Dehaine does not teach the invention as claimed in claim 1. Specifically, Dehaine fails to disclose or suggest that the complementary chip’s first face is physically attached to the active face of the active chip. Dehaine also fails to disclose or suggest the dimensional characteristics of the recesses specified in claim 1 (*i.e.*, that the recesses extend in height through the entire thickness of the complementary chip, and extend transversely from above a contact terminal to a side surface of the complementary chip).

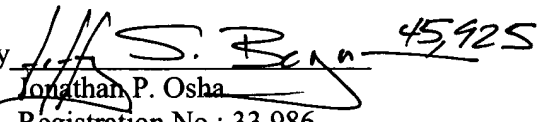
Further, as claim 5 includes similar allowable subject matter, and APA does not specify that which Dehaine lacks (*i.e.*, APA does not disclose or suggest the placement of the complementary chip and active chip faces or the dimensions of the recesses on the complementary chip recited in claim 1), claim 5 is patentable over Dehaine and APA, whether considered separately or in combination. Further, dependent claims 6-7 are patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 09669/005001; 76.0562US).

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Respectfully submitted,

By  45925
Jonathan P. Osha
Registration No.: 33,986
Osha & May L.L.P.
1221 McKinney, Suite 2800
Houston, Texas 77010
(713) 228-8600
(713) 228-8778 (Fax)